QSFP28-112G-ER4

112Gbps QSFP28 Transceiver, Single Mode, 40km Reach

Product Features

- Supports 100GBASE (103.1Gb/s) and OTU4 (111.8Gb/s) aggregate;
- Lane bit rate 25.78 Gb/s 100GE, 27.95Gb/s OTU4;
- Up to 40km transmission on SMF;
- LAN WDM EML laser and APD receiver;
- High speed I/O electrical interface (CAUI-4);
- I2C interface with integrated Digital Diagnostic monitoring;
- QSFP28 MSA package with duplex LC connector;
- Single +3.3V power supply;

- Maximum power consumption 5 W;
- Operating case temperature: 0 to +70 °C;
- Compliant to SFF-8665 and SFF-8679;
- Complies with EU Directive 2011/65/EU (RoHS 6/6);

Application

- 100GBASE-ER4

Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	T_S	-40	-	+85	°C	
Supply Voltage	V_{CC}	-0.5	-	+4.0	V	
Operating Relative Humidity	RH	-	-	+85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	T_C	0	-	+70	°C	
Power Supply Voltage	V_{CC}	3.13	3.3	3.47	V	
Power Supply Current	I_{CC}	-	-	1.5	A	
Maximum Power Dissipation	P_D	-	-	5	W	
Aggregate Bit Rate	BR_{AVE}	-	103.125	-	Gb/s	
Lane Bit Rate	BR_{LANE}	-	25.78	-	Gb/s	
Transmission Distance	TD		-	40	km	Over SMF

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Center Wavelength Lane 0	λ_0	1294.53	1295.56	1296.59	nm	
Center Wavelength Lane 1	λ_1	1299.02	1300.05	1301.09	nm	
Center Wavelength Lane 2	λ_2	1303.54	1304.58	1305.63	nm	
Center Wavelength Lane 3	λ_3	1308.09	1309.14	1310.19	nm	
Total Launch Power, 100GE	P_{ALL}	-	-	12.5	dBm	1
Average Launch Power per Lane, 100GE	P_{TX_LANE}	-2.5	-	6.5	dBm	1
OMA per Lane, 100GE	OMA	0.5	-	6.5	dBm	1
Average Output Power (Laser Turn off)	$P_{0UT-OFF}$	-	-	-30	dBm	
Difference in launch power between lanes	$P_{TX\_DELTA\_LANE}$	-	-	4	dB	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Extinction Ratio, 100GE	ER	4.5	-	-	dB	
Launch power in OMA minus TDP, per lane	OMA - TDP	-0.5	-	-	dBm	
Transmitter and Dispersion Penalty	TDP	-	-	3	dB	2
Transmitter reflectance	Tref	-	-	-26	dB	
Optical Return Loss Tolerance	ORLT	20	-	-	dB	
Optical Eye Mask, 100GE	Compliant with 4WDM-40 MSA {0.25, 0.4, 0.45, 0.25, 0.28, 0.4}					2
Receiver						
Center Wavelength Lane 0	λ_0	1294.53	1295.56	1296.59	nm	
Center Wavelength Lane 1	λ_1	1299.02	1300.05	1301.09	nm	
Center Wavelength Lane 2	λ_2	1303.54	1304.58	1305.63	nm	
Center Wavelength Lane 3	λ_3	1308.09	1309.14	1310.19	nm	
Damage threshold	Pdamage	-	-	-2.5	dBm	
Average Rx Power per Lane, 100GE	P_{RX_LANE}	-20.5		-3.5	dBm	3
OMA Sensitivity per Lane, 100GE	P_{OMA_LANE}	-	-	-18.5	dBm	3
Reflectance	Ref	-	-	-26	dB	

Stressed receiver sensitivity (OMA), per lane,100GE	SRS	-	-	-16	dBm	
Conditions of stressed receiver sensitivity test						
Vertical eye closure penalty per lane		2.5			dB	
Stressed eye J2 Jitter per lane		0.33			UI	
Stressed eye J9 Jitter per lane		0.48			UI	
SRS eye mask definition { X1, X2, X3, Y1, Y2, Y3}		{0.39, 0.5, 0.5, 0.39, 0.39, 0.4}				

Notes:

1. The optical power is launched into SMF.
2. Measured with a PRBS 2^{31}-1 test pattern @25.78125 Gb/s, Hit ratio≤5E-5.
3. Measured with a PRBS 2^{31}-1 test pattern @25.78125 Gb/s, BER≤5E-5.

Electrical Characteristics

High-Speed Signal: Compliant to CAUI-4 (IEEE 802.3bm)

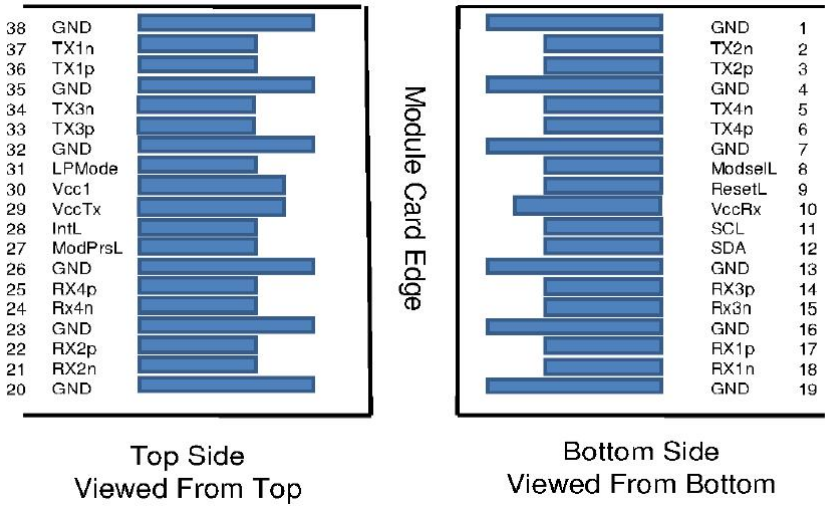
Low-Speed Signal: Compliant to QSFP-8679.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter (Module Input)						
Differential Data Input Amplitude	$V_{IN,P-P}$	85	-	900	mVpp	
Differential Termination Mismatch		-	-	10	%	
LPMode, Reset and ModSelL, V in low	V_{IL}	-0.3	-	0.8	V	
LPMode, Reset and ModSelL, V in high	V_{IH}	2.0	-	V_{CC}+0.3	V	
Receiver (Module Output)						
Differential Data Output Amplitude	$V_{OUT,P-P}$	200	-	900	mVpp	
Differential Termination Mismatch		-	-	10	%	
Transition time, 20% to 80%	Tr Tf	12			ps	
ModPrsL and IntL, V out low	V_{OL}	0	-	0.4	V	
ModPrsL and IntL, V out high	V_{OH}	V_{CC}-0.5	-	V_{CC}+0.3	V	

Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to V_{CC}	0.1	V	Internal
Tx Bias Current Per Lane	0 to 100	10%	mA	Internal
Tx Output Power Per Lane	-2.5 to 6.5	±3	dBm	Internal
Rx Power (Each Lane)	-20.5 to -3.5	±3	dBm	Internal

Pin Definitions



Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

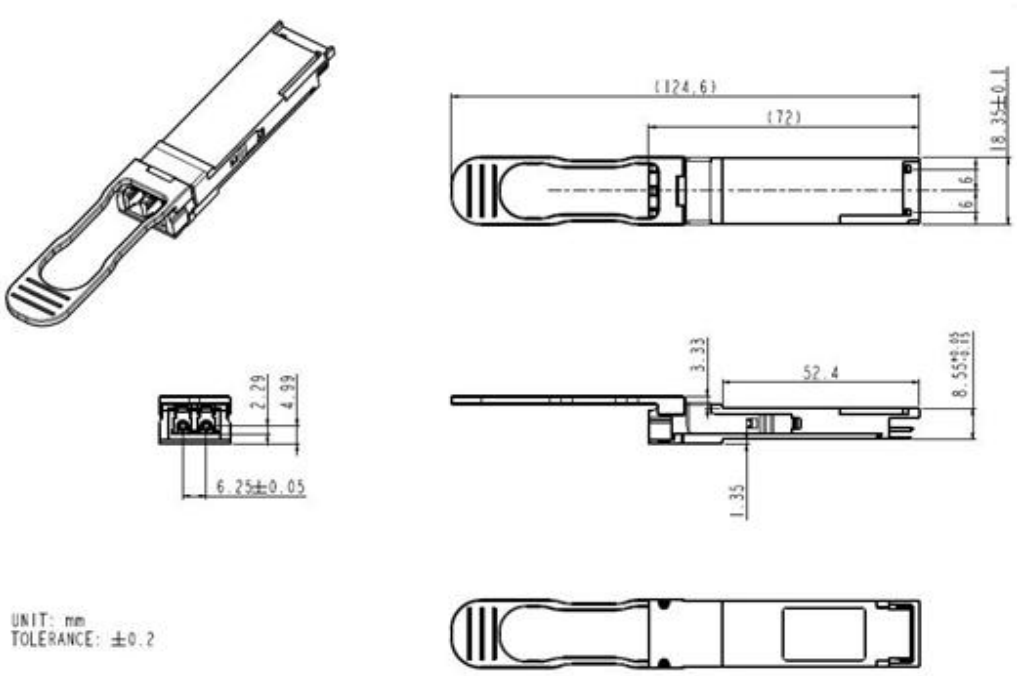
PIN	Logic	Symbol	Description	Plug Seq.	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	3	
7		GND	Ground	1	1
8	LVTLL-I	ModSelL	Module Select	3	
9	LVTLL-I	ResetL	Module Reset	3	
10		VccRx	+ 3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3	
13		GND	Ground	1	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1

27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		VccTx	+3.3 V Power Supply transmitter	2	2
30		Vcc1	+3.3 V Power Supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Output	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Output	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in MSA. The connector pins are each rated for a maximum current of 1000 mA.

Mechanical Dimension



Ordering Information

Part Number	Product Description
QSFP28-112G-ER4	1310nm, 112Gbps, LC, 40km, 0°C~+70°C, with DDM