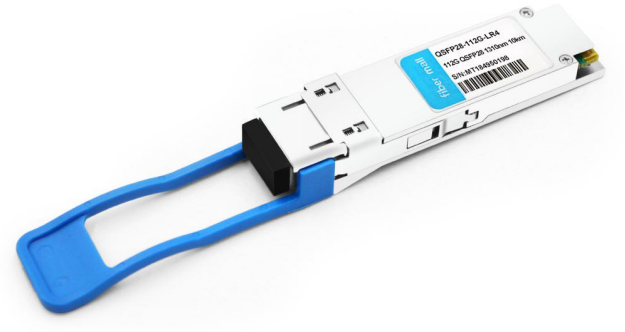
QSFP28-112G-LR4

112Gbps QSFP28 Transceiver, Single Mode, 10km Reach



Product Features

- Supports multi-rate (100GBASE 100GE and OTU4); from 103.1Gb/s to 111.8Gb/s aggregate;
- Lane bit rate 25.78 Gb/s 100GE, 27.95 Gb/s OTU4;
- Up to 10km transmission on SMF;
- LAN WDM DML laser and PIN receiver;
- High speed I/O electrical interface (CAUI-4);
- I2C interface with integrated Digital Diagnostic monitoring;
- QSFP28 MSA package with duplex LC connector;

- Single +3.3V power supply;
- Support HW TX_DIS and RX_LOS for telecom application;
- Maximum power consumption 3.5 W;
- Operating case temperature: 0 to +70 °C;
- Compliant to IEEE 802.3bm, SFF-8665 and SFF-8679;
- Complies with EU Directive 2011/65/EU (RoHS 6/6);

Application

- 100GBASE-LR4

Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	T_S	-40	-	+85	°C	
Supply Voltage	V_{CC}	-0.5	-	+4.0	V	
Operating Relative Humidity	RH	-	-	+85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	T_C	0	-	+70	°C	
Power Supply Voltage	V_{CC}	3.13	3.3	3.47	V	
Power Supply Current	I_{CC}	-	-	1.1	A	
Maximum Power Dissipation	P_D	-	-	3.5	W	
Aggregate Bit Rate	BR_{AVE}	-	103.125	-	Gb/s	
Lane Bit Rate	BR_{LANE}	-	25.78	27.952	Gb/s	
Transmission Distance	TD		-	10	km	Over SMF

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Center Wavelength Lane 0	λ_0	1294.53	1295.56	1296.59	nm	
Center Wavelength Lane 1	λ_1	1299.02	1300.05	1301.09	nm	
Center Wavelength Lane 2	λ_2	1303.54	1304.58	1305.63	nm	
Center Wavelength Lane 3	λ_3	1308.09	1309.14	1310.19	nm	
Total Launch Power, 100GE	P_{ALL}	-	-	10.5	dBm	1
Average Launch Power per Lane, 100GE	P_{TX_LANE}	-4.3	-	4.5	dBm	1
OMA per Lane, 100GE	OMA	-1.3	-	4.5	dBm	1
OMA–TDP per Lane, 100GE	OMA_TDP	-2.3	-	-	dBm	
Difference in launch power between lanes	$P_{TX\_DELTA\_LANE}$	-	-	3.6	dB	
Total Launch Output Power, OTU4	P_{ALL}	-	-	10	dBm	1
Average Launch Power per Lane, OTU4	P_{TX_LANE}	-0.6	-	4	dBm	1
Average Output Power (Laser Turn off)	$P_{0UT-OFF}$	-	-	-30	dBm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Extinction Ratio, 100GE	ER	4	-	-	dB	
Transmitter and Dispersion Penalty	TDP	-	-	2.2	dB	2
Optical Return Loss Tolerance	ORLT	-	-	20	dB	
Optical Eye Mask, 100GE	Compliant with IEEE 802.3bm					2
Optical Eye Mask, OTU4	Compliant with ITU-T G.959.1					2
Receiver						
Center Wavelength Lane 0	λ_0	1294.53	1295.56	1296.59	nm	
Center Wavelength Lane 1	λ_1	1299.02	1300.05	1301.09	nm	
Center Wavelength Lane 2	λ_2	1303.54	1304.58	1305.63	nm	
Center Wavelength Lane 3	λ_3	1308.09	1309.14	1310.19	nm	
Average Rx Power per Lane, 100GE	P_{RX_LANE}	-10.6		4.5	dBm	3
OMA Sensitivity per Lane, 100GE	P_{OMA_LANE}	-	-	-8.6	dBm	3

Average Rx Power per Lane, OTU4	$P_{RX\_AVE\_LANE}$	-6.9		4	dBm	3
Sensitivity per Lane, OTU4	$P_{\_OMA\_LANE}$	-	-	-8.4	dBm	3
Receiver Overload	P_{IN-OL}	4.5	-	-	dBm	
Reflectance	Ref	-	-	-26	dB	
LOS Assert per lane	LOS_A	-20	-	-	dBm	
LOS De-assert	LOS_D	-	-	-12	dBm	
LOS Hysteresis	LOS_H	0.5	-	4	dB	

Notes:

1. The optical power is launched into SMF.
2. Measured with a PRBS 2^{31}-1 test pattern @25.78125/27.952 Gb/s, Hit ratio≤5E-5.
3. Measured with a PRBS 2^{31}-1 test pattern @25.78125 Gb/s, BER≤1E-12.
4. Measured with a PRBS 2^{31}-1 test pattern @27.952 Gb/s, BER≤1E-12(with FEC), BER≤1E-6(Pre-FEC).

Electrical Characteristics

High-Speed Signal: Compliant to CAUI-4 (IEEE 802.3bm)

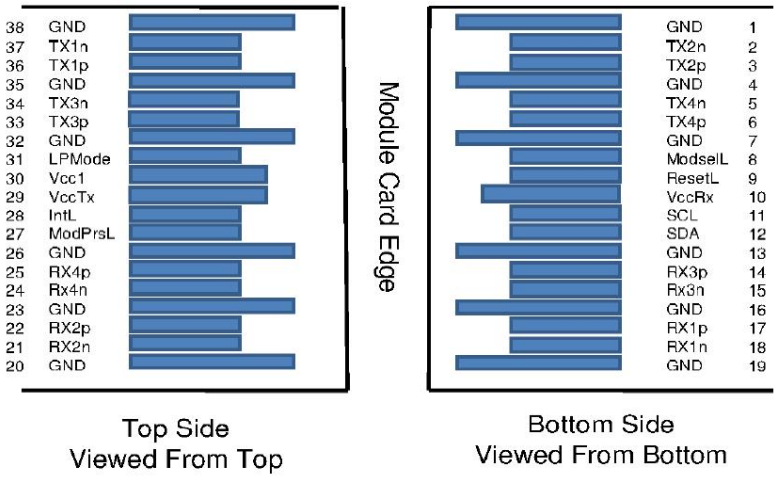
Low-Speed Signal: Compliant to QSFP-8679.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter (Module Input)						
Differential Data Input Amplitude	$V_{IN,P-P}$	85	-	900	mVpp	
Differential Termination Mismatch		-	-	10	%	
LPMode, Reset and ModSelL / Tx dis	V_{IL}	-0.3	-	0.8	V	
LPMode, Reset and ModSelL / Tx dis	V_{IH}	2.0	-	V_{CC}+0.3	V	
Receiver (Module Output)						
Differential Data Output Amplitude	$V_{OUT,P-P}$	200	-	900	mVpp	
Differential Termination Mismatch（1MHZ）		-	-	10	%	
Output Rise/Fall Time, 20%~80%	T_R	12	-	-	ps	
ModPrsL and IntL / Rx los	V_{OL}	0	-	0.4	V	
ModPrsL and IntL / Rx los	V_{OH}	V_{CC}-0.5	-	V_{CC}+0.3	V	

Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to V_{CC}	0.1	V	Internal
Tx Bias Current Per Lane	0 to 100	10%	mA	Internal
Tx Output Power Per Lane	-4.5 to 5	±3	dBm	Internal
Rx Power (Each Lane)	-15 to 5	±3	dBm	Internal

Pin Definitions



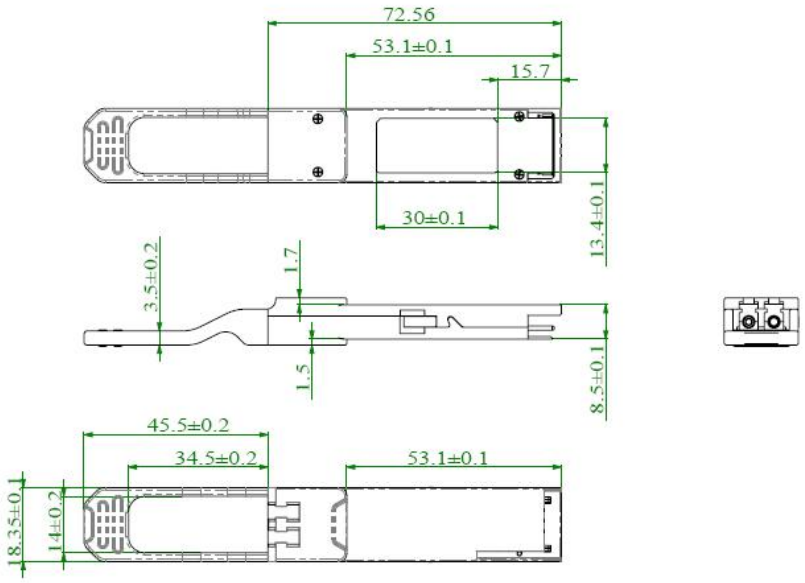
PIN	Logic	Symbol	Description	Plug Seq.	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	3	
7		GND	Ground	1	1
8	LVTLL-I	ModSelL	Module Select	3	
9	LVTLL-I	ResetL	Module Reset	3	
10		VccRx	+ 3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3	
13		GND	Ground	1	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	

28	LVTTL-O	IntL/Rx Los	Interrupt / Rx los output	3	
29		VccTx	+3.3 V Power Supply transmitter	2	2
30		Vcc1	+3.3 V Power Supply	2	2
31	LVTTL-I	LPMode/Tx dis	Low Power Mode / Tx disable input	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Output	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Output	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in MSA. The connector pins are each rated for a maximum current of 1000 mA.

Mechanical Dimension



Ordering Information

Part Number	Product Description
QSFP28-112G-LR4	1310nm, 112Gbps, LC, 10km, 0°C~+70°C, with DDM